Simulation and Evaluation of Time Synchronization Performance Based on NTP and PTP

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Summary—**For the study and evaluation of NTP and PTP time synchronization performance, a simulation tool was constructed, to simulate the time synchronization process of NTP and PTP. The tool does not depend on any network simulator, and models detailedly the node, the time transfer link and the taming algorithm. Some NTP and PTP time synchronization cases were designed and implemented based on the simulation tool. Preliminary conclusions are obtained based on the referenced real parameters of time transfer links and the typical node clock specification. ADEV of the slave node in the four-hop network is an order of magnitude bigger than that of a direct connection network. Larger taming period can bring worse time synchronization performance, even the slave clock cannot achieve the tamed state. The clock with worse performance can cause TDEV and ADEV of the slave node increase by two orders of magnitude.**

Keywords—NTP; PTP; simulation model; time synchronization performance

I. INTRODUCTION

Network Time Protocol (NTP) and IEEE 1588-2008 Precision Time Protocol (PTP) are two commonly used network time synchronization technology based on packets exchange. There have been some former studies on building simulation models and analyzing the time synchronization performance of NTP and PTP. An NTP simulator described in [1] is used to simulate and study the process of NTP. However, it only considers the total network delay, and is not able to describe the delay of the router that mainly causes the round-trip transmission path asymmetry in detail. Some simulation models for PTP were built in [2]-[5]. References [3] and [4] analyzed the influence of time synchronization interval and path asymmetry on time synchronization performance with their models. But the simulation models built in [2]-[5] depended on some network simulators (such as OMNeT++ and NS-3) and did not cover all the main factors that affect the time synchronization performance.

In this paper, all the main factors, such as clocks, timestamps, and round-trip transmission path asymmetry in the time synchronization process of NTP and PTP, were studied and described by the mathematical models. Based on the models, a simulation tool was constructed, which does not depend on any network simulator.

II. MODEL DESCRIPTION

From the principles of time synchronization, both NTP and PTP use four receiving and sending timestamps of the client and the server to calculate the path delay and the time difference. Thanks to the similarity, the factors in the time synchronization process of NTP and PTP can be analyzed simultaneously. As shown in Fig. 1, the time synchronization simulation model is built by modeling the main factors, including the clock-related error, the timestamp-related error, the path delay, and a PID controller. The PID controller is used to adjust the slave node to realize time synchronization.

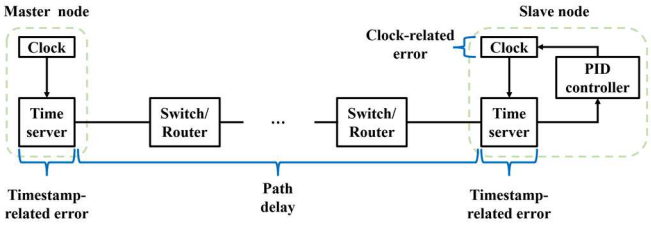


Fig.1 The structure of the simulation model

A. Clock-related Error

The clock-related error is represented by the clock model, which has been investigated in [6]. The clock is generally an oscillator, which is an electronic device composed of electronic components, including noise from the electronic components. Over a period of time, the time difference of the clock can be divided into the system part and the random part. The system part contains the factors such as linear frequency drift and daily trend changes. The random part can often be characterized by power law spectra. For an NTP or PTP time synchronization system, the clock in the master node called the master clock, is considered to be accurate as the global reference, and the slave clock synchronizes its time to that of the master clock. t is the global reference time in the time synchronization system. The time difference model of the master clock at time t is given by (1).

$$M(t) = 0 \tag{1}$$

The time difference model of the clock in the slave node at time t can be described as (2).

$$S(t) = S_0 + a_0 \cdot t + \frac{1}{2} b_0 \cdot t^2 + \varepsilon(t) \qquad (2)$$

S_0 and a_0 are the time difference and the frequency difference at initial time $t = 0$, respectively. b_0 represents the linear variation of frequency difference, often referred to as aging or frequency drift. $\varepsilon(t)$ is the clock random noises, which is typically characterized by one or more of the various power law processes. The five random noises that typically affect clock signals are white phase modulation (WPM), flicker phase modulation (FPM), white frequency modulation (WFM), flicker frequency modulation (FFM), random walk frequency modulation (RWFM). According to (1) and (2), the time difference of the slave clock from the master clock at time t can be obtained as $S(t)$.

B. Timestamp-related Error

Almost any clock may be considered a two-part device. The first part is an oscillating device, which determines the length of the second or some other desired time interval. The second part is a counter, which keeps track of the number of seconds or clock cycles that have occurred[7]. Obviously, there is an update interval for the counter, during which the clock face time does not change. It leads to a random error between the time captured by the timestamp and the continuous real time. In this paper, this random error is defined as the timestamp reading error. Fig.2 describes the timestamp reading error.

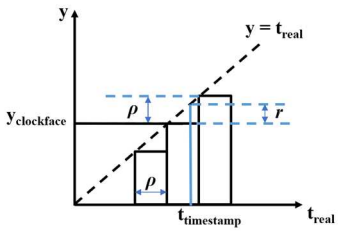


Fig.2 Schematic diagram of timestamp reading error

The abscissa represents continuous real time t_{real}, and the ordinate represents clock face time y. ρ is the update interval for the counter. The clock face time captured by the timestamp at real time $t_{\text{timestamp}}$ is $y_{\text{clockface}}$, and the difference between clock $t_{\text{timestamp}}$ and $y_{\text{clockface}}$ is r, defined as the timestamp reading error. Reading the timestamps continuously can be regarded as the process of independent identically distribution, so r obeys a uniform distribution in the interval [$-\rho$,0].

Fig.3 shows the NTP and PTP sending timestamps generation model. The NTP timestamp is generated in the application layer. From obtaining the timestamp to being sent to the network, the data packet needs to go through the protocol stack, including the application layer, the transport layer, the network layer, the data link layer and the physical layer. The protocol stack introduces delays for some factors, such as the First In First Out queue of the network interface card and interrupt response. These delays also exist when the receiving timestamp is generated. In [8], the standard uncertainty of error of time difference of client caused by the NTP timestamps was evaluated as 2.5 ms. With the assistance of hardware, the layer where the PTP timestamp is generated is moved to the Media Independent Interface. This method of timestamp generation introduces only nanoseconds of hardware latency. Random numbers from a Gaussian distribution are used to describe protocol stack delays for a series of timestamps of the node as [9] does.

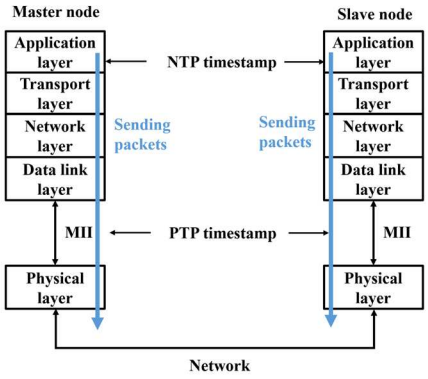


Fig.3 NTP and PTP sending timestamps generation model

C. Path Delay

NTP and PTP synchronization principles are based on the assumption that the forward and backward path delays are equal. With the traffic load and the complex structure of the network, this assumption doesn't work most of the time. According to [10], in the case of stable routing, queuing delay results in Packet Delay Variation (PDV), and an intermediate device (such as a router or a switch) in the network is an independent M/M/1 queue. Therefore, theoretically, the cumulative queuing delay of packets passing through a series of intermediate devices obeys the Gamma distribution. Assuming that the route is stable, and setting the one-way delay of the data packet network to D. The network delay $D[i]$ (i represents the packet index) for a series of data packets transmitted from one node to another node is written as (3).

$$D[i] = C + P[i] \qquad (3)$$

C is a constant and is the sum of all fixed delays. $P[i]$is the queuing delay of the i-th data packet and is described as a series of random numbers obeying the Gamma distribution.

D. Clock Taming Operation

Compensating the time difference of the slave clock from the master clock directly may cause large time jumps. In this paper, a PID controller is implemented in the slave node for frequency difference compensation, which is written as (4).

$$u(t) = k_p e(t) + k_i \int e(t)\, dt + k_d \frac{de(t)}{dt} \qquad (4)$$

$u(t)$ is the output of the PID controller. $e(t)$ is the frequency difference, which can be calculated by the time difference. k_p, k_i and k_d are the parameters of the proportional controller, the integral controller and the derivative controller respectively.

III. CASES STUDY

Based on the models in section Ⅱ, a simulation tool was constructed, which supports the simulation of NTP and PTP time synchronization processes. The tool is a self-developed software and does not depend on any network simulator. The node clock, time transfer link, the parameters of the PID controller and the clock taming period can be set. In this section, for the study of time synchronization performance, the influence of time transfer link, clock taming and controlling and node clock are analyzed with some typical simulated cases.

A. Time Transfer Link

A network hop is defined that a router or a switch that a packet passes from its source to its destination. Considering that PTP can use transparent clocks and boundary clocks to mitigate the path asymmetry, the NTP simulation case was used to analyze the impact of hop count on time synchronization. The accuracy of the slave node clock was 10 ppm. The hop count increased from zero (master and slave nodes are connected directly by a network cable) to eight. The delay of each switch in the forward path and backward path came from an exponentially distributed sequence with a mean of 0.5 ms. Path asymmetry was described by the standard deviation of the difference between the forward and backward path delays. TABLE Ⅰ presents the asymmetry of different hop counts. Asymmetry with 0.1 μs accuracy because the ρ was set to 0.1 μs. The delay asymmetry that still exists was caused by the timestamp-related error of the master node and the slave node.

TABLE I. THE ASYMMETRY OF THE PATH DELAY FOR DIFFERENT HOP COUNTS

Network hop count	Asymmetry
Direct connection	100.2 μs
One-hop	706.7 μs
Four-hop	1400.4 μs
Eight-hop	1995.4 μs

Fig.4 and Fig.5 present the Allan deviation (ADEV) for all averaging time and ADEV for averaging time 101s of the slave node with different hop counts. More hop counts lead to worse frequency stability. From direct connection to four hops, ADEV increases by an order of magnitude. The maximum increment of ADEV value corresponds to the change from direct connection to one hop, which is close to an order of magnitude.

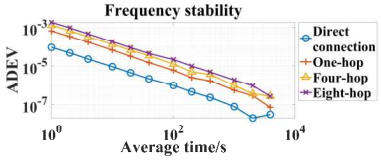


Fig.4 Frequency stability and of the slave node

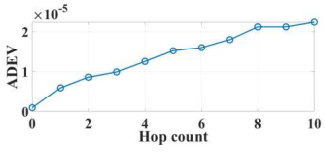


Fig.5 ADEV@101s with different hop count

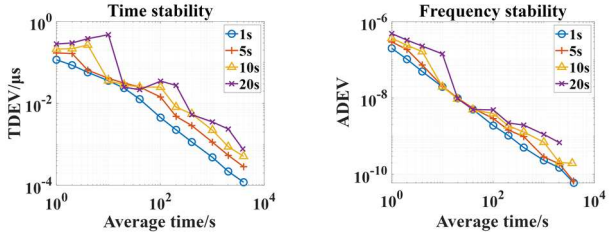
B. Clock Taming and Controlling

The sampling interval $\Delta t_{oboffset\_interval}$ for the time difference between the master node and the slave node based on NTP or PTP may not be equal to the clock taming period (i.e. clock adjustment interval) Δt_{tame_period}. To study the effect of different taming periods on time synchronization performance, $\Delta t_{oboffset\_interval}$ was set to 1 s, and Δt_{tame_period} increased from 1 s. In this case, the parameters of the PID controller were unchanged and the time difference between the master node and the slave node was obtained by PTP. The accuracy of the slave node clock was 10 ppm. There were 8 switches with transparent clock functions between the master node and the slave node. The moment of taming convergence was defined as the initial moment when the time difference did not exceed t_{CM} μs and remained for more than 50 s. t_{CM} which was determined empirically was different with taming periods.

TABLE II. CONVERGENCE MOMENT AT DIFFERENT TAMING PERIODS

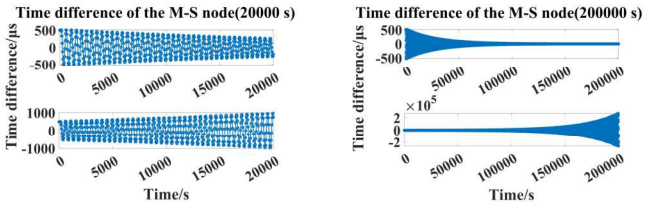
Δt_{tame_period}	Convergence moment
1 s	165 s
5 s	840 s
10 s	1700 s
20 s	4500 s

TABLE Ⅱ shows the convergence moment at the different taming periods. Fig 6.(a) and Fig 6.(b) present the time stability and the frequency stability of the slave node after convergence respectively. The above and below pictures in Fig.7(a) are the time difference curve when Δt_{tame_period} was 36 s and 37 s. The simulation duration was 20000 s. It can be seen that when Δt_{tame_period} was 37 s, the time difference curve showed a divergent shape. By increasing the simulation duration to 200000 s with Δt_{tame_period} was 37 seconds, the time difference curve diverges more significantly.



(a) (b)

Fig.6 Time stability and frequency stability of the slave node



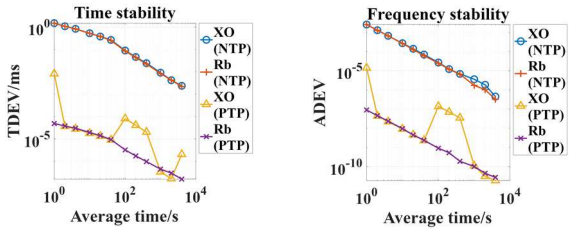
(a) (b)

Fig.7 Time difference of the master node and the slave node

The cumulative error of the slave clock increases as the taming time interval became larger. The larger the taming time interval, the more inaccurate the prediction of the PID controller and the larger the residual error after frequency compensation. This is reflected in the TDEV and ADEV increase. Moreover, the time differences become divergent and the slave clock could not achieve the tamed state. Therefore, the clock taming period needs to be considered carefully and an appropriate reduction of the taming period can bring better time stability and frequency stability.

C. Node Clock

The simulation tool is able to build the model of the slave clock based on (2). The simulation duration was 20000 s. The slave clock was set to a typical Crystal Oscillator (XO) or a typical rubidium atomic clock. The frequency difference and the drift of the XO were 10^{-6} and10^{-11}/day, respectively. The frequency difference and the drift of the rubidium atomic clock were 5×10^{-10} and 10^{-11} /month, respectively. $\Delta t_{oboffset\_interval}$ and $\Delta t_{tame_interval}$were set to 1 s and 2 s.



(a) (b)

Fig.8 Time stability and frequency stability of the slave node

Fig.8(a) and Fig.8(b) present the time stability and the frequency stability of the slave node after time synchronization. Time differences are obtained more accurately by PTP than by NTP due to the smaller noise of time transfer link. From the results when the slave node clock was a rubidium atomic clock, TDEV and ADEV of the slave node based on PTP time synchronization are both four orders of magnitude smaller than those of NTP. For the results of NTP time synchronization, the effect of the node clock on time synchronization performance is not obvious whether the slave node clock was XO or a rubidium atomic clock. For the results of PTP time synchronization, TDEV and ADEV for averaging time 1 s, 100 s, 200 s and 400 s of the XO were two orders of magnitude bigger than those of the rubidium atomic clock. The relatively larger frequency difference of the XO leads to a larger cumulative error. As the analysis in case B, there was a larger residual after frequency compensation. The clock with worse performance deteriorates time synchronization. This indicates that both time transfer link and the node clock should be considered to achieve better time synchronization performance.

IV. Conclusions and Outlook

In this paper, the main error sources that affect NTP and PTP time synchronization performance are discussed and a simulation tool that supports the simulation of NTP and PTP time synchronization processes is constructed. The influence of different factors on time synchronization performance was analyzed. Preliminary conclusions are obtained based on the referenced real parameters of time transfer links and the typical node clock specification. (1) Time synchronization performance based on NTP deteriorates most significantly when the network environment changes from direct connection to one-hop. From direct connection to four hops, ADEV will increase by an order of magnitude. (2) Larger taming period can bring worse time synchronization performance. In our experiment, the slave clock cannot achieve the tamed state when the taming period was 37 s. (3) Both time transfer link and node clock should be considered. The clock with worse performance can cause TDEV and ADEV of the slave node increase by two orders of magnitude and deteriorates time synchronization performance. In the future, we will conduct research on the time scale algorithms and the ensemble time to analyze the performance of NTP and PTP time synchronization based on the simulation tool.

Acknowledgment

This work was supported by the National Key R&D Program of China with grant no. 2021YFB3900704 and 2021YFB3900701.

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